Abstract of the Disclosure:

A semiconductor substrate is provided, on which there is arranged a first layer, a second layer and a third layer. The third layer is, for example, a resist mask that is used to pattern the second layer. The second layer is, for example, a patterned hard mask used to pattern the first layer. Then, the third layer is removed and a fourth layer is deposited. The fourth layer is, for example, an insulator that fills the trenches which have been formed in the first layer. Then, the fourth layer is planarized by a CMP step. The planarization is continued and the second layer, which is, for example, a hard mask, is removed from the first layer together with the fourth layer. The fourth layer remains in place in a trench which is arranged in the first layer.

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